Collaborative Research: NSF CISE Medium Propopsal: Stochastic Resonance Decoders for Information Transmission and Storage Systems

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The goal of the proposed research is to establish a comprehensive theoretical framework as well as to implement this new paradigm for information transmission and storage. Not only will our correction circuits be fault-tolerant, but randomness will make these decoders superior to perfect correction circuits. Even more interesting is that such useful random perturbations do not require any additional hardware – they are built in the noisy hardware itself.

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Project Summary

Motivation: *Stochastic resonance* – the phenomenon that noise can be used constructively and enhance the performance of a system – has been observed in many of natural and engineered analog signal processing systems, with a neuronal noise in nervous systems as a prime example. Recently, we have discovered the same phenomenon in some iterative decoding algorithms for codes on graphs, and found a way to make a noisy decoder capable of correcting *more* errors than a "perfect" decoder made of noiseless logic gates. While our initial findings indicate rather impressive improvements, precise mechanisms underlying this behavior are far from being understood. Since generation of noise requires no hardware resources – noise is generated in the normal operation of decoder's logic, especially when when gates operate in the low-power regime – huge energy savings and/or clock speed improvements are possible. We propose to investigate methods of improving performance of decoders by means of noise in the decoder and to devise hardware aware decoding algorithms for optimally exploiting stochastic resonance mechanisms. In particular, we will explore applications of the above framework in resistance-switching memristors by exploiting their inherent randomness.

We will study the dynamics of noisy decoding algorithms and establish its relation to particle methods used in statistical physics as well as genetic algorithms, simulated annealing, stochastic gradient descent and other non-deterministic optimization methods. Our boldest goal is to approach the maximum-likelihood (ML) performance limit by simple noisy decoders. A third objective of the proposed effort is to develop low-complexity and low power consumption hardware solutions superior to the existing ones used in storage and communications channels.

Intellectual Merit: The proposed paradigm shift consists of relying on extremely simple node processors and improving decoding convergence by noise that is inherently present in processors. Using the large body of knowledge in coding theory and VLSI design gained in the past decade will allow us to design novel decoders based on this framework. The depth and generality of results we aspire to obtain call for collaborative research well beyond capabilities of individual research groups. We propose to leverage a unique combination of expertise involving international collaborators in information and coding theory and VLSI design. Together with our experience in applications in data storage, electronic technologies, low power signal processing and data communications, the combined expertise of our international partnership provides our team with an ability to tackle this complex problem.

Broader Impacts: This program will contribute significantly to the evolution of data storage and communications technologies by tracing a path to a new generation of data storage systems that will reduce greatly the energy requirements and lower their impact on the environment. A second anticipated impact is in communications systems, where our noise-enhanced algorithms can offer high performance signal processing with a greatly reduced power budget. An important component of this project are our French collaborators. In terms of collaborative educational impacts, the University of Arizona already has a dual graduate degree program with University of Cergy-Pontoise, France, and we envision similar agreements with Université de Bretagne-Sud, which is also involved in this project. The proposed research will help our continued effort in involving underrepresented students into research in partner universities, facilitate exchange of students and faculty. Highly competent workforce produced this way will contribute to the competitiveness of US industry especially in the strategically important areas of data storage and green communications.

Key words Coding theory; LDPC codes; iterative decoding; fault-tolerance.

Project Description

With the steady increase of integration density offered by nano-technologies, the main technological obstacle to overcome is to develop a non-determinisitic computing paradigm beyond the legacy of von Neumann, Turing, and Boole that will embrace the inherent stochastic behavior of nano devices and circuit fabrics. Traditional architectures and current error-correction coding schemes are incapable of handling such randomness, thus novel sophisticated error correction systems are required.

Stochastic resonance is a well established phenomenon in neural systems, lasers, semiconductor and quantum interference devices. It has been exploited computationally in image processing, detection, parameter estimation and search algorithms, but until now there has been little success in applying these methods in the domain of error-correction decoders. In the past two years, the PIs made major advances in this direction. Our results show that stochastic resonance decoding algorithms can have exceptional performance and very low resource cost, and may prove superior to established techniques in many applications. These results came as a surprise as the PIs were seeking decoders that would *tolerate* internal upsets, but found algorithms that are *enhanced* by those faults, with performance improved by orders of magnitude. We now seek to understand the mechanisms beneath noise enhancement, so that this phenomenon may be optimized and harnessed for its full benefit in error-correction applications.

We propose to initiate a collaboration between Utah State University (USU) and the University of Arizona (UA) to study noise-enhanced error correction algorithms, with application to reliable data storage and low-power data communication systems. This project will merge the PIs' previously independent activities, which recently converged on similar results that point toward a common set of new research challenges and objectives. Initially, our main focus will be on an important class of error correction methods, the Low Density Parity Check (LDPC) codes, which play a role in a growing range of standards. As our research progresses, we will expand attention to spatially coupled codes, Reed-Muller and finite geometry codes and their decoding algorithms that can benefit from stochastic resonance.

Error correction decoders form an integral part of most high-performance data storage and communication systems, from Flash memories to ethernet networks. These are tightly constrained applications which demand very efficient resource utilization by the decoder. In order to make real progress in hardware efficiency it is necessary to design algorithms with a strong *hardware awareness*. Modern decoders traditionally require complex signal processing and can consume a sizable fraction of a system's total power budget. In order to reduce energy cost and environmental impact, there is a constant motive to reduce the power consumption and operating voltage of these devices, which degrades noise margins and increases the likelihood of internal logic upsets or timing errors, thereby making fault tolerance all the more important .

In addition to improving decoding efficiency in conventional CMOS technologies, we consider the rapidly developing field of "post-CMOS" nano-scale devices, where non-deterministic behavior is inevitable. In the proposed work, we will address this class of technologies generally, and will also give specialized attention to resistance-switching memristors as a case-study in stochastic computing. Memristors form the basis of resistive RAM (ReRAM) technologies and nano-scale cross-bar logic. Several major companies have invested heavily in this technology [1, 2], but commercial deployment of large-scale memristive systems has not kept pace with the advance in research. Researchers are now investigating memristors for implementing classical stochastic computation [3]. This style of computing uses random Bernouli sequences to emulate arithmetic

functions. It is a highly fault-tolerant solution, and has been well studied in the field of error correction [4–6], including prior research by Winstead [W1–W3]. In this project, we propose to go beyond classical stochastic computing and exploit **stochastic resonance**. We will leverage non-deterministic switching not merely for emulation but *as a computational asset* that will greatly improve the system-scale performance of this technology.

Philosophy of our approach Recent research has shown that stochastic resonance decoding can equal or exceed the performance of traditional deterministic Belief Propagation (BP) and related message passing (MP) algorithms. During the past two years, the PIs independently discovered two stochastic resonance bit-flipping (BF) algorithms with surprisingly good performance that can approach or surpass BP in many cases [W4], [V1]. These results are significant because BF requires very simple arithmetic compared to BP-based algorithms, and can feasibly be integrated into a wider range of resource-constrained applications. Furthermore, since these algorithms are assisted by noise, they are inherently fault tolerant. In short, **probabilistic behavior within a decoder due to unreliable components can be exploited for improved performance and energy efficiency with reduced hardware redundancy.**

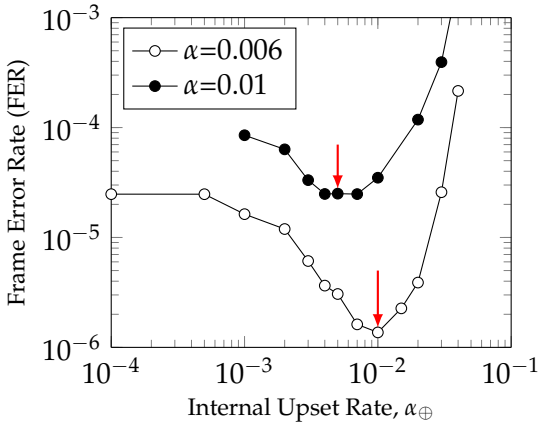


Figure 1: Noise enhancement in a Gallager-B decoder. The optimal performance, indicated by arrows, requires a moderately high rate of random internal upsets in the decoder.

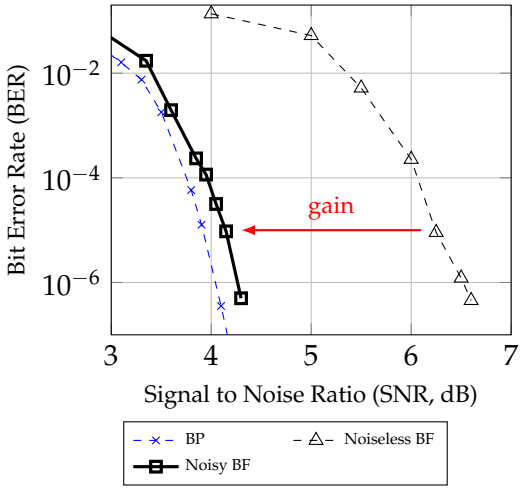


Figure 2: Noise enhancement in a bit-flipping decoder for a 10Gb ethernet standard. Noise perturbations yield 2dB of gain and approaches BP performance. With multi-phase BF decoding, the performance equals BP.

Motivating Example 1: Fig. 1 shows results for the well-known Gallager-B algorithm which consists of only of two types of logic gates: majority logic (MAJ) gates and XOR ($\oplus$) gates. The decoder is used to correct upsets in a solid-state memory that occur with rate α, and the decoder itself experiences internal parity upsets with rate $\alpha_{\oplus}$. The decoder's performance is measured via its Frame Error Rate (FER), which is traditionally expected to be a monotonic function of the quality parameters α and $\alpha_{\oplus}$. Surprisingly, the best FER is not obtained by the "perfect" noiseless decoder. Indeed, for the case where $\alpha = 0.006$, the FER is improved by more than an order of magnitude when the decoder has frequent internal upsets, at $\alpha_{\oplus} = 0.01$. This behavior points toward a new approach in stochastic computation, with particular benefits for memristive logic and other post-CMOS nano-devices, and other technologies where the non-deterministic switching probability can be tuned by changing circuit parameters.

Motivating Example 2: Fig. 2 shows the performance of a very simple noisy BF decoding algorithm. The original BF algorithm has poor performance, but when perturbed by noise, the performance becomes almost equal to that of the presumably optimal BP algorithm. The BF decoder offers

extraordinary advantages: gate area is 5× lower than a BP-based decoder, and the energy efficiency is improved by more than 4× (further details are given in Sec. 2.1). The resulting decoder architectures are very promising for communications and computing technologies, where they can improve energy efficiency without sacrificing performance.

Preliminary Work: Up to now, PIs Winstead and Vasic have been pursuing these topics independently. During 2014, our respective teams converged on very similar solutions based on the Gradient Descent Bit Flip (GDBF) decoding algorithm. Winstead's team developed a Noisy GDBF (NGDBF) algorithm [W4] for use on Gaussian channels, in collaboration with researchers in Brittany, France. Vasic's team developed a Probabilistic GDBF (PGDBF) algorithm for use on binary symmetric channels (BSC) [V1], in collaboration with researchers in Cergy-Pontoise, France. In 2015, we initiated an informal collaboration to open communication between all parties working on these methods. We published a series of papers that have convinced us in importance of further study of this class of decoders: [V2–V11] (a brief overview of our preliminary results are given in Section 1). Most recently, our French colleagues received a 1.5 Million Euro grant from the Agence Nationale de la Recherche (ANR-15-CE25-0006-01), and this project includes more than twelve French institutions from both academia and industry. With this proposal, we plan to deepen that collaboration and address the harder questions posed by our results.

Open problems The initial results raise a number of challenging research problems outlined below and discussed in depth in the rest of the proposal. In order to truly tap the benefits of our novel algorithms, we need to better understand why they work so well and how they can be optimized. We will organize our research around the following topics:

1. The first question is whether stochastic resonance is a unique property of the PIs' recently discovered algorithms, or do other iterative decoding algorithms exhibit similar resonance under appropriate conditions? More generally, what is a common feature of codes and decoding algorithms that makes them robust, and how can this robustness be analytically determined for a given decoder architecture?
2. From the theoretical side, the dynamics of noisy decoding algorithms may be related to particle methods [7] used in statistical physics as well as genetic algorithms [8], simulated annealing and other non-deterministic optimization methods. Up to now, we have not identified a clear correspondence between stochastic resonance decoding and generalized optimization frameworks. We will conduct a deeper investigation to either explain our algorithms in terms of an existing framework, or define a new framework that will likely have broader applications to other optimization domains.
3. Our recent experiments and insights in iterative decoding dynamics partially explain behavior of stochastic resonance decoders: since iterative decoding can be viewed as a recursive procedure for minimizing the Bethe free energy function, random perturbations in message updates may help the decoder escape from local minima. It has been established that the local minima of iterative decoders can be attributed to the presence of some small subgraphs, known as *trapping sets*, present in the Tanner graph of a code. These subgraphs make the perfect decoder fail to converge, but they appear to be less harmful for the noisy decoder. While the above observation is intriguing, it raises a number of difficult questions. For one thing, we do not yet precisely understand the mechanism of escaping from these harmful subgraphs, or how to optimize the escape process for practical applications.

4. Gate failures are correlated and data-dependent, which greatly complicates the analysis. We will establish theoretical bounds on error correction capability of a range of codes and decoding algorithms in the presence of dominant failures, such as timing data-dependent errors.
5. Our decoders will exhibit error floors at lower error rates than conventional algorithms. While this is an extremely valuable attribute, low error floors are exceptionally difficult to measure. To accelerate these measurements, we will develop an FPGA decoding architecture with on-board channel emulation.
6. Proper tuning of the gate reliability, depending on their function within the decoder, can lead to tremendous savings in energy consumption. This concept therefore opens completely new directions in energy efficient decoder design. We will develop circuits and architectures for decoding with controlled randomness in post-CMOS nano-devices. As a representative model, we will consider memristor circuits based on established cross-bar topologies. Using available stochastic models of memristor switching, combined with typical current/voltage profiles of their switching behavior, we will be able to forecast the tradeoffs in energy and reliability with memristor-based decoders.
7. Another open question pertains to the limits of BF decoders, which are not amenable to the asymptotic analyses used for BP-based algorithms. In one significant case, we are able to show that noise-assisted BF decoding approaches the maximum-likelihood (ML) performance limit, which is superior to the limits of conventional BP-based decoders. This result motivates further study.
8. Due to large graphs, our stochastic resonance setting is much more complex than the existing ones and the available analysis. Novel theoretical interpretations and analysis methods will be sought, which may prove useful both for our direct objectives and for the broader field of research in noisy computation.

1 Background

Prior work

In the context of iterative decoding of LDPC codes, the first trace of a randomized iterative algorithm can be found in Gallager's work where the random flips are used to resolve ties in the majority voting operation in the variable node, while the first iterative decoding algorithm that explicitly relies on randomness to correct errors is Probabilistic Bit Flipping (PBF) [9]. A closely related technique of adding noise to messages in a BP decoder on the AWGN channel is by Leduc-Primeau *et al.* [10] for reducing error floors. These positive effects of noise are also observed in early analog decoders where randomness comes from transistor mismatch [11]. Randomness in a message update schedule [12] is also observed to yield improved convergence of iterative decoders.

The main feature of the existing work on noisy decoders is a focus on the analysis of the existing decoder types and demonstrating their robustness to unreliability of logic gates [13–18] (We discuss the analysis approaches in Section 2.3.) This was also the underlying idea of our prior work [V12, V13], [W2]. On the contrary, the idea of the proposed work is to allow randomness in a decoder in order to improve convergence in the spirit of stochastic approximation methods [19, 20].

More specifically, we were able to show in [W4] and [V1] that random perturbations can be used to increase the performance of a gradient descent bit flipping decoder (GDBF), introduced

by Wadayama *et al.* [21]. At the same time we observed that the randomness coming from computational noise even more improves the GDBF decoding performance. Our preliminary work includes exploring: (i) approaching ML decoding by noisy GDBF [V2],(ii) error floor and convergence speed analysis [V3], (iii) data dependent gate failure model [V4], (iv) expander arguments for data-dependent gate failures [V5], (v) FPGA hardware for PGDBF [V6], (vi) importance of irregular gate reilabilities [V7], (vii) concept of rewinding of noisy decoders [V8], (viii) fault-resilient decoders and memories [V9], (ix) analysis and efficient hardware implementation of PGDBF [V10], (x) noisy one-step majority logic decoder [V11]. **For all noisy decoders that we have studied, we observed similar FER performance improvements in both waterfall as well as in error floor for codes of various lengths and rates.**

We emphasize that the concept of randomness in a decoder is novel, and is not related to the existing decoding algorithms such as "stochastic decoders" [4,5,22] which also rely on randomness but in a very different way — by representing messages as random sequences with a given probability distribution [W2]. Note also that the simulated annealing method is used for code graph layout optimization as well as to provide dynamic scheduling of message passing. These decoders are designed to emulate the traditional BP algorithm and cannot outperform their deterministic counterparts. Stochastic decoders are also negatively impacted by the deterministic constraints within the Tanner graph [W1], which has proved to be a major limitation in their development.

It has been well demonstrated that very long binary LDPC codes perform nearly to the Shannon limit when considering very long codeword length [23]. But they suffer from a reduction in performance when the code word length is small or moderate, or when higher order modulation is used for transmission. A proposed solution to this issue is the extension of binary LDPC codes to Galois Fields $(GF(q))$ with $q > 2$ or nonbinary LDPC codes [24] which in comparison to binary LDPC code, offers better communication performance. However, this performance gain comes with the cost of increasing decoding complexity. As the size of $GF(q)$ increases, the decoding difficulty increases significantly and a straightforward implementation of the BP algorithm has a complexity of $O(q^2)$ [25,26]. In recent years several works have been proposed to reduce the decoding complexity in non-binary LDPC code without hampering communications performance. Declercq *et al.* [27] addressd the problem of decoding nonbinary LDPC codes over finite fields $GF(q)$ with reasonable complexity and proposed a simplified decoder named extended min-sum (EMS) inspired from the conventional min-sum decoder for binary LDPC codes. They have have tried to demonstrate that the computational complexity of the check-node processing can be reduced by computing approximate reliability measures with a limited number of values in a message. Voicila *et al.* [26] has also proposed an Extended Min-Sum (EMS) decoder for non-binary LDPC code with a truncated message of the decoder in order to reduce decoding complexity and memory requirements. Li *et al.* [28] proposed a modification of the EMS algorithm where they show a new way to compute modified configuration sets, using a trellis representation of incoming messages to check and demonstrate that the new trellis representation reduces the computational complexity without any hampering the performance. Bocharova *et al.* [29] estimated on the error probability of the maximumlikelihood (ML) decoding over an AWGN channel with BPSK signaling for short codes from different ensembles of LDPC codes and concluded that ML decoding performance should not be used as a target for searching for good iteratively decodable codes. By using the existing bounding techniques, estimates on the error probability of the maximumlikelihood (ML) decoding over an AWGN channel with BPSK signaling for short codes from different ensembles of LDPC codes are obtained. The numerical results show performance of the ML decoding for

different code ensembles. Some recent works has addressed the necessity for efficient hardware architectures for non binary LDPC code implementation because the state-of-the-art decoding algorithms lead to architectures with low throughput and high latency. Schläfer *et al.* [30] has proposed hardware aware check node algorithm for high throughput hardware implementations in the future. Zhang *et al.* [31] also proposed a highly parallel LDPC decoder design for the (2048,1723) RS-LDPC code suitable for 10GBASE-T Ethernet where they have used a two-step decoding scheme in order to shorten the minimum wordlength required for good decoding performance and the message-passing decoding is scheduled on a 7-stage pipeline to deliver a high throughput. All these recent works pave the way that there are scopes in improving the decoding complexity of non binary LDPC code. At the same time we need to solve the the practical issue of building a suitable decoder that can be easily configurable in hardware without compromising the performance. It has been also observed that, all the prior work in decoding of non binary LDPC code, most of the cases researchers focused on soft decoders such as Beleif Propagation message passing algorithm or ML decoding, or List Decoding. Which also inspires us to explore hard decoding algorithm performance in case of non binary LDPC code such bit flipping algorithm or syndrome based bit flipping algorithm.

Before we proceed to outline the main directions of the proposed research and specific goals, we introduce iterative decoders of LDPC codes and noisy message update functions.

1.1 LDPC codes and decoding algorithms

LDPC codes and iterative decoding: Let $\mathcal{C}$ be an (N, K) binary LDPC code of rate $R = K/N$, and let $\mathbf{x} = (x_1, x_2, \ldots, x_N)$ denote a codeword of $\mathcal{C}$ transmitted over a discrete output memoryless channel, resulting in the received vector $\mathbf{y} = \{y_1, y_2, \ldots, y_N\}$,which is decoded by an iterative decoder $\mathcal{D}$. At the ℓ-th iteration ($\ell \in [0, L]$, where L is the maximal number of iterations), the decoder produces the estimated codeword $\hat{\mathbf{x}}^{(\ell)}$.

Logic operations as well as any storage of intermediate variables within a decoder are also subject to errors, as we describe shortly. A decoding failure is said to occur if the error pattern is uncorrectable by a decoder after L iterations.

To ensure the redundancy is linear in word length and to reduce the error propagation in a decoder due to faulty gates, we consider a general class of message-passing and bit-flipping decoding algorithms. They operate on G, a Tanner graph of a code, consisting of the set of N variable nodes and the set of M check nodes . The parity check matrix H of the code $\mathcal{C}$ is the bi-adjacency matrix of G. The decoding algorithm consists of sending messages between variable nodes v corresponding to code bits and check nodes, c corresponding to parity check equations in which the variables (bits) are involved in (see Fig. 3).

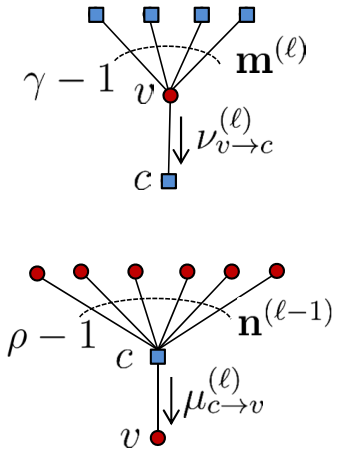


Figure 3: Node update functions. Variable nodes are represented by circles, and check nodes by squares. A circle is connected to a square if a variable is involved in the parity check equation corresponding to a square.

General framework for noisy message-passing decoders: We consider $\mathcal{D}$, an $|\mathcal{M}|$-level finite alphabet iterative decoder (FAID) [V14], defined as a 5-tuple $\mathcal{D} = (\mathcal{M}, \mathcal{Y}, \Phi, \Psi, \hat{\Phi})$. The message values are confined to a finite alphabet $\mathcal{M}$. $\mathcal{Y}$ denotes the channel output alphabet. For mathematical convenience we choose $\mathcal{Y} = \{\pm C : C \in \mathbb{Z}^+\}$. By convention, for the binary symmetric channel (BSC) $+C$ corresponds to

the input 0 and $-$C to 1. $\Psi : \mathcal{M}^{\rho-1} \to \mathcal{M}$ is the update function used at a check node with degree ρ. $\Phi : \mathcal{Y} \times \mathcal{M}^{\gamma-1} \to \mathcal{M}$ is an update rule used at a variable node with degree γ. $\hat{\Phi}$ is the variable node decision function.

Let $v_{v\to c}^{(\ell)}$ denote the message passed by a variable node $v \in V$ to its neighboring check node c in the ℓ^{th} iteration and let $\mu_{c\to v}^{(\ell)}$ denote the message passed by a check node c to its neighboring variable node v. The messages are computed according to the following *noisy update rules*.

$$\begin{aligned} v_{v\to c}^{(\ell)} &= \Phi(y_v, \mathbf{m}^{(\ell)}) + e_{\Phi}^{(\ell)} \\ \mu_{c\to v}^{(\ell)} &= \Psi(\mathbf{n}^{(\ell-1)}) + e_{\Psi}^{(\ell)}. \end{aligned}$$

$\mathbf{m}^{(\ell)}$ denotes the incoming messages to a variable node v except a message from the check node c, and $\mathbf{n}^{(\ell)}$ are all incoming messages to the check node c except from variable node v. The $e_{\Phi}^{(\ell)}$ and $e_{\Psi}^{(\ell)}$ are errors/noise due to faulty computation of the (deterministic or "perfect") update functions Φ and Ψ and storing the intermediate result in a register until the next iteration. They are modeled as random variables taking values in the message alphabet $\mathcal{M}$. For Gallager A/B algorithms, the messages and errors are binary.

Extended framework for APP and BF algortihms: Noisy *a postierior* probability (APP) decoders with quantized likelihoods and multi-bit BF decoders such as [V15] can be defined similarly. As opposed to message passing decoders the APP decoders iteratively update variable nodes v based on $\mathbf{i}^{(\ell)} \in \mathcal{M}_C^{\gamma}$, the messages incoming to v in the ℓ-th iteration, and check nodes c based on $\mathbf{a}^{(\ell)} \in \mathcal{M}_V^{\rho}$, the messages incoming to c in the ℓ-th iteration. Note that the alphabets $\mathcal{M}_C$ and $\mathcal{M}_V$ for check and variable node messages are different, and typically $|\mathcal{M}_C| \ll |\mathcal{M}_V|$. For gradient-descent type algorithms, the update of the variable node message $v_v^{(\ell)}$ also involves Δ, an n-tuple of variable node "inverse functions." A variable node inverse function tracks the number of neighboring satisfied checks and their likelihoods.

$$\begin{aligned} v_v^{(\ell)} &= \Phi(y_v, \mathbf{i}^{(\ell)}, \Delta) + e_{\Phi}^{(\ell)} \\ \mu_c^{(\ell)} &= \Psi(\mathbf{a}^{(\ell-1)}) + e_{\Psi}^{(\ell)}. \end{aligned} \tag{1}$$

where now $\Psi : \mathcal{M}_V^{\rho} \to \mathcal{M}_C$ is the update function used at a check node with degree ρ. $\Phi : \mathcal{Y} \times \mathcal{M}_C^{\gamma} \times \mathcal{M}_C^{n(\rho+1)} \to \mathcal{M}_V$ is an update rule used at a variable node with degree γ. (For the sake of conciseness, we refer the reviewers to [21], [V1] and [W4] more details on Δ).

The noise/error distributions may be defined in several different ways. For the sake of brevity, the discussion and examples provided in the proposal are for binary decoders on the BSC, and a simple von Neumann or *independent error model*, e_{Φ} and e_{Ψ} as well as the memory element errors are independent Bernoulli random variables. In the proposed research we will consider more general data-dependent error models as discussed in Section 2.4.

2 Objectives

Up to now, our research on stochastic resonance algorithms has been largely heuristic, and we are here proposing to tackle the deeper problems of how these algorithms work and how they can be fully exploited. In order to tackle the open research problems previously described, we will pursue a number of detailed technical objectives described in this section.

2.1 Novel stochastic gradient-descent decoding algorithms

In this research avenue we will investigate iterative BF and MP algorithms for the BSC and AWGN channels. The basis for development of new algorithms in this research avenue serves our probabilistic gradient-descent bit flipping algorithm (PGDBF) [V1] for the BSC.

The key concept that will be explored in this research is the inversion function defined as [21, Eqn. (6)]

$$\Delta_v^{(\ell)}(\hat{\mathbf{x}}, \mathbf{y}) = \chi_v^{(\ell)} \eta_v + \sum_{c \in \mathcal{N}_v} \prod_{u \in \mathcal{N}_c} \chi_u^{(\ell)}. \tag{2}$$

where $\boldsymbol{\eta} = (-1)^{\mathbf{y}}$ and $\boldsymbol{\chi}^{(\ell)} = (-1)^{\hat{\mathbf{x}}^{(\ell)}}$ denote the "bipolar" versions of the received word $\mathbf{y}$ and codeword estimate $\hat{\mathbf{x}}^{(\ell)}$. The algorithm includes initializing a variable node v to $\chi_v^{(0)} = \eta_v$, and calculating $\Delta_v^{(\ell)}$ in the ℓ-th iteration. The concept of the inversion is introduced to provide a local measure of invalidness of the current variable node estimate based on the neighboring checks [21].

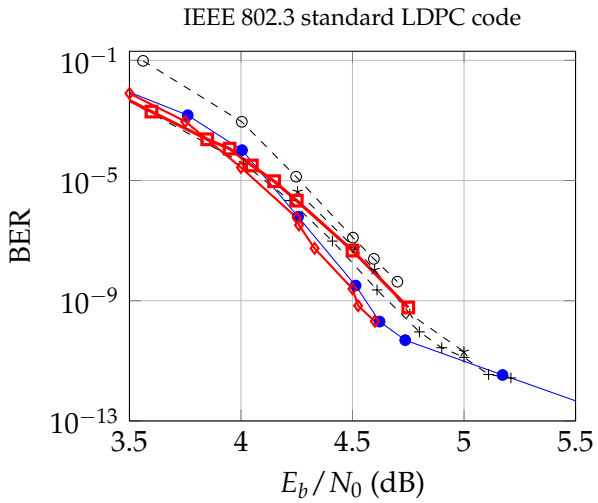
The classical GDBF algorithm by Wadayama *et. al* [21] prescribes deterministic rules for bit flipping based on the flipping function $\Delta_v^{(\ell)}$. Our PGDBF introduces a random perturbation in v in each iteration ℓ, conditional on $\Delta_v^{(\ell)}$, while NGDBF similarly introduces a Gaussian perturbation on $\Delta_v^{(\ell)}$, followed by a threshold operation to determine v. With these modifications, it is possible to construct much better decoding algorithms. Our initial results show that some specific algorithms are capable of escaping from a local maximum of the objective function. This practically means that noisy version of GDBF *breaks trapping sets* of the deterministic GDBF, and in the proposed research we will investigate this behavior with a goal to design better algorithms.

Initial results on NGDBF performance and implementation Winstead's group has completed a demonstration design targeted for the IEEE 802.3an 10GBase-T ethernet standard. This standard uses a $(2048, 1723)$ Reed-Solomon based LDPC code. Several integrated circuit (IC) decoders have been reported for this standard, all in similar 65 nm technologies, making it a well-suited case for benchmarking the practical applicability of new algorithms. Fig. 4 shows the comparative bit error rate (BER) performance along with a comparison of IC results. **We found that NGDBF performs equally to traditional message-passing decoders, but uses about $5\times$ less gate area, and has about $5\times$ better energy efficiency.** Since the area is so low, we can also consider using parallel decoders to improve speed and/or performance. A double-decoder case is shown in Fig. 4.

In these results, traditional BP-based decoder designs (SRMS and OMS) are able to come within 0.2 dB of BP. The NGDBF decoder achieves similar performance. A competing bit-flipping method, called "Improved Differential Binary" (IDB), was developed contemporaneously with NGDBF and is also shown [32]. The IDB has efficiency close to NGDBF, but our experience has found that IDB is not as robust when applied to other codes. We will nevertheless include IDB in benchmark comparisons throughout our proposed research.

2.2 Noisy ML-approaching iterative decoders

Recently Vasic's group has been studying ML approaching performance of PGDBF and FAID decoders under the framework described in Sec. 1.1. For a given code we found a set of FAIDs is capable of correcting errors not correctable by individual decoders in the set [V16, V17]. Moreover, we found that this so called **decoder diversity** technique is ML approaching when the decoder set is large (9,236 distinct decoding rules in [V17]). It is interesting that ML-approaching performance



Design:	**NGDBF**	IDB [32]	SRMS [33]	OMS [34]
Area (mm^2)	**0.82**	1.44	4.84	5.35
Power (mW)	**63**	478	1359	-
Clock (MHz)	**189**	520	195	700
Av Tp (Gbps)	**36.4**	171.8	92.8	-
EpB (pJ/bit)	**1.73**	2.78	8.64	40.8

Figure 4: Performance comparison of 802.3an decoders. BP represents the best obtainable performance under message passing, limited to 12 iterations on a 6-bit quantized AWGN channel. Practical (sub-optimal) performance benchmarks for Split-Row Min-Sum (SRMS) and Offset Min-Sum (OMS) are shown. The recent IDB bit-flipping algorithm is also shown, along with our results for NGDBF. A table comparing implementation results is shown, where each design was implemented for the 802.3an standard using a 65 nm CMOS technology.

can be achieved with such a simple algorithm (here "simple" refers to the implementation area, power consumption and average energy efficiency rather than the time complexity).

In the proposed work, we will build on the idea that decoder diversity is inherently present in a single noisy decoder (both MP and BF type decoders). Moreover, different decoders can be obtained simply, by changing supply voltage of some gates in the decoder, thus modifying gate failure rate and consequently the decoding dynamics. This points toward not only an explanation noise enhancement, but by studying diversity in FAIDs it may be possible to prescribe optimal perturbation sets for noisy decoders.

Similar conclusions hold for PGDBF on the BSC and AWGN. On short-length LDPC codes, like the Tanner $(155, 64, 20)$ code, PGDBF is able to achieve performance similar to BP. One of our unusual findings with PGDBF is that its performance can approach that of a maximum likelihood (ML) decoder if given a high iteration limit, as shown in Fig. 5. ML performance is in general very difficult to achieve with iterative decoding algorithms. PGDBF achieves similar performance by allowing more time to complete "hard-to-decode" frames. Due to the early stopping condition, the vast majority of frames complete after just a few iterations, with an average of less than ten iterations when $\alpha = 0.02$. We confirmed that the error events at low α are dominated by minimum-distance errors, which implies that PGDBF is able to resolve trapping sets if given sufficient time.

2.3 Decoding dynamics

Markov chain framework: Characterization of the FER performance of a given noisy decoder $\mathcal{D}$ requires computing the probability $\Pr\{\hat{\mathbf{x}}^{(\ell)} \neq \mathbf{x}\}$ for different channel error vectors $\mathbf{e}$ and finding its dependence on the parameters $\alpha_{\oplus}$, α_{MAJ} and L. The goal is to find a region in a parameter space in which $\mathcal{D}$ outperform their noiseless counterpart $\overline{\mathcal{D}}$.

Let $\boldsymbol{\mu}^{(\ell)} = (\mu_c^{(\ell)})_{c \in C}$ be the ordered set of all messages from check nodes in iteration ℓ. From Eq. (1), they can be expressed as $\boldsymbol{\mu}^{(\ell)} = \Upsilon_C(\boldsymbol{\mu}^{(\ell-1)}) + \mathbf{e}_{\boldsymbol{\mu}}^{(\ell)}$, where the function Υ_C is the composition of Φ and Ψ, and define the dynamical system of the noiseless decoder. The binary vector $\mathbf{e}_{\boldsymbol{\mu}}^{(\ell)}$ of

length $n\gamma$ ($= m\rho$) is the realization of errors at time ℓ that affect the computation of messages $\boldsymbol{\mu}$. In [V3], we found a condition under which the random process $\{\boldsymbol{\mu}^{(\ell)}\}_{\ell>0}$ is a homogenous Markov chain with finite state space.

Using the above method on the entire code graph is computationally demanding, but fortunately, our initial investigation in [V3] indicates that that it can be simplified and applied to specific code subgraphs corresponding to most harmful error patterns (trapping sets of $\overline{\mathcal{D}}$) while keeping its accuracy.

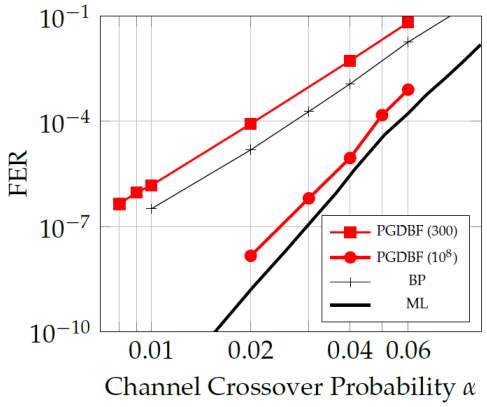


Figure 5: Performance of PGDBF for the (155,64) Tanner code on the BSC.

Convergence speed: Due to randomness in a decoder, it is clear that there is nonzero probability of reaching an all-zero syndrome at ℓ-th iteration, and halting decoding (the Markov chain above is absorbing). The key is to design a decoder so that the gate errors direct the decoding trajectory quickly towards the correct codeword before the gate errors combined with channel errors overwhelm the decoder's correction capability. It is important to note that while approaching the ML performance requires large number of iterations or multiple decoders working in parallel, stochastic resonance decoders have a potential of outperforming their noiseless counterparts even in small number of iterations.

Fig. 6, show the average FER as a function of L for the Tanner (155,64) code. The impact of the parameters $\alpha_{\oplus}$ and α_{MAJ} can be condensed to a single parameter (denoted by α_G, where G stands for "gate").The best curve corresponds to the *rewinding* schedule in which decoder is reinitialized after L_R iterations. Our intuition is that it minimizes the negative effects of gate failures because it prevents accumulation of errors in large number of iterations, thus resulting in a faster performance improvement. In the proposed research this effect will be analytically quantified.

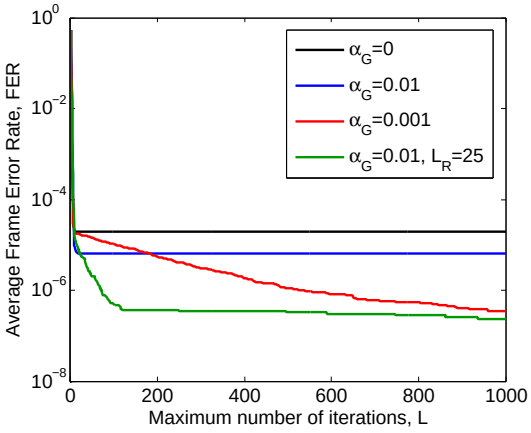


Figure 6: The FER performance of the noisy Gallager-B decoder as a function of number of iterations on the Tanner (155,64) code for $\alpha = 5 \times 10^{-3}$. The noisy decoder outperforms the perfect one after only $L = 10$ iterations, while after $L = 30$ iterations, the FER is almost two orders of magnitude better.

Exploration and absorbtion: As we mentioned in the introduction, besides the PGDBF, the Gallager B decoder with unreliable majority logic gates (MAJ) such that $\alpha_{MAJ} \ll \alpha_{\oplus}$ also exhibits the similar behavior. Although studied under unrealistic logic gate noise assumption, the Min-Sum decoder was also observed to benefit from noise [18]. The second insight is that the *irregularity* of gate reliability plays a crucial role here. Randomness in computing parity checks is a way of "exploring" various possible trajectories (defined as a time evolution of messages), while the more reliable MAJ computation and minimization of the modified inverse function eliminate some of these trajectories and guides the decoder to one converging to a correct codeword. This suggests a connection with genetic algorithms [8]. and interacting particle methods [7] as discussed in the following

paragraphs. Introducing a memory in the GDBF update rule, will be equivalent to the particle (variable) evolution phase, and our intuition is that it will improve convergence. However, the tradeoffs among resulting complexity increase, logic gate reliability and probability of selecting a wrong trajectory need to be investigated.

Stochastic resonance analytic tools: Due to large graphs, our stochastic resonance setting is much more complex than the existing ones for example in signal processing, and the available analysis tools are not applicable. In this research novel stochastic resonance interpretations and analysis methods will be sought, which may prove useful both for our direct objectives and for the broader field of research in stochastic resonance.

The relation of the Belief Propagation (BP) algorithm to the Bethe free energy (BFE) minimization has been established in [35] and studied thoroughly in recent years (see for example [36–39]). The fixed points of BP correspond to the stationary points of the BFE. While in a tree-like graph the BFE is a concave function, in a loopy graph, local minima are present leading to oscillation and multiple fixed points. When the BP is used to compute the marginals of codeword symbols on (loopy) Tanner graphs, these local minima are responsible for decoding failures. We have explored these minima and corresponding graphical structures in a series of papers [V18–V22]. Various variational methods that are aware of the BFE local structure are proposed in both statistical physics and machine learning literature.

The probability distribution of the trajectories in the underlying Markov process driven by the decoding algorithm, weighted by the "potential functions" corresponding to the absorbing states (codewords) forms a Feynman-Kac measure [7, Chpt. 3]. The fact that a decoder explores a random decoding trajectory and converges to a codeword is equivalent to the exploration/killing mechanism in the interacting particle methods setting [7].

The second research avenue is understanding connections with stochastic gradient descent algorithms. Using gradient descent method as a decoding algorithm dates back to Farrell *et al.* [40]. The BP based algorithms and APP decoding algorithm are also special cases of the gradient descent algorithm as shown in Lucas *et al.* [41] and noted in [42]. In our work, the concept of the inversion function provides a local measure of invalidness of the current variable node estimate based on the neighboring checks. By introducing a logic condition under which a random perturbation $\Delta_v^{(\ell)}$ is applied to variable v in each iteration ℓ, we were able to construct a decoder capable of escaping from a local maximum of the objective function, wherein the objective function corresponds to the correlation between a codeword estimate and the received word and can be viewed as an energy of a system [21].

2.4 Performance limits

Recent developments: Formulating a general method for construction of robust stochastic resonance decoders requires understanding if a particular decoder is inherently robust to errors. To answer this question, Varshney [13] introduced a framework referred to as noisy Density Evolution (noisy-DE) for the performance analysis of noisy LDPC decoders in terms of asymptotic error probability. Based on this framework, the asymptotic performance of a variety of noisy LDPC decoders was analyzed. In [13], infinite precision BP decoders were investigated, which are not suitable for actual implementation on faulty hardware. On the contrary, hard-decision decoders, such as noisy Gallager-A and Gallager-E decoders were recently considered in [13] and [14]. Gallager-B decoders were also analyzed for binary [V12, V13], [15] and non-binary [16] alphabets under

transient error models, and [14] also considered permanent error models. From the same noisy-DE framework, [17,18] proposed an asymptotic analysis of the behavior of stronger discrete Min-Sum decoders, for which the exchanged messages are no longer binary but are quantized soft information represented by a finite (and typically small) number of bits. Dupraz *et. al* [V23] analyzed faulty FAID decoders.

Functional region of a decoder: In this research avenue, we will develop a rigorous method for the analysis and design of decoding rules robust to transient errors introduced in the decoder. Some initial results are presented in [V23], where we used noisy-DE for computing thresholds of faulty finite alphabet decoders. The conceptual difficulty is that the decoder's inability to correct errors is caused by a complex interplay of gate faultiness and decoder's suboptimality. Another issue is that at high level of gate unreliability, the threshold effect might not be present.

Data-dependent gate errors: In addition to von Neumann type of errors [43], other error mechanisms from the Pippenger's ϵ-admissible failure model class [44,45] will be studied. The independent and adversarial failure models are only a rough approximation of the physical processes leading to logic gate failures. The actual probability of failure of logic gates is highly dependent on a digital circuit manufacturing technology. For high integration factors the failures are data dependent and/or temporally correlated, as was shown by Zaynoun *et al.* [46]. For example, timing errors are heavily dependent on data values processed by the gate in previous bit intervals and cannot be represented accurately by the von Neumann model. For data-dependent adversarial failure models, we will provide provable guarantees such that a given memory architecture can tolerate a constant fraction of failures in all the components.

2.5 Energy efficiency and hardware complexity assessment

Conventional ASIC and FPGA technologies: Winstead's team has substantial experience with hardware-level design, analysis, synthesis and testing of error correction decoders. This experience has helped us identify algorithm features that promote good hardware efficiency, leading to the excellent results shown in Fig. 4. We now propose to apply these methods in an expanded effort to understand noise enhancement and how it can improve efficiency in conventional hardware implementations. In concert with the theoretical investigations described above, we will develop efficient architectures to demonstrate newly optimized stochastic resonance algorithms and benchmark them against the state of the art.

In the context of conventional architectures, we will use our existing design framework to aid algorithm analysis and improvements, and to perform rigorous benchmarking of novel stochastic resonance algorithms using standard synthesis/place-and-route (SPR) flows applied to ASIC and FPGA targets, where we can precisely evaluate the gate complexity, energy efficiency, throughput, latency and performance of hardware designs. Where applicable, we will work within the specifications of established standards, like the 802.x family, for which there are ample hardware results in the literature that can serve as benchmarks for our work. In addition to our analysis of algorithm dynamics, we will consider the cost and performance tradeoffs associated with several sources of noise perturbations, including traditional pseudorandom noise, harvesting randomness already present in the channel information, circuit-level noise generation from true random number generators, "hard-wired" samples computed at design time, and the effect of sample reuse in order to minimize the need for random generation events.

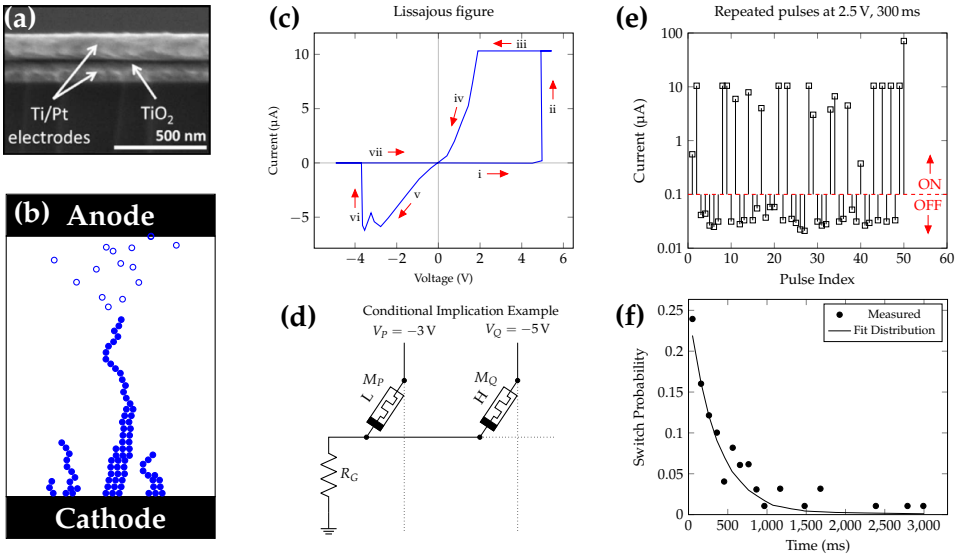


Figure 7: Overview of memristive devices: (a) Typical thin-film fabrication (photo from [50]). (b) Physical mechanism of stochastic resistance switching via ion migration and formation of a dominant filament [51]. (c) "Pinched hysteresis" figure showing abrupt resistance switching at steps ii and vi, corresponding to applied voltages of $\pm 5\,\mathrm{V}$ [52]. (d) Cross-bar circuit for implication-based logic, where M_Q is supposed to be unchanged due to inadequate switching voltage [53]. (e) Stochastic switching at sub-threshold voltages, where device states are reset by a strong negative voltage between each pulse [52]. (f) Observed probability density of switching as a function of time [52]; about 23% of pulses cause switching within the first 100 ms interval, 16% during the 100–200 ms interval, and so on. The distribution can also be tuned by changing pulse amplitude.

Memristive technologies: Looking beyond conventional technologies, we will explore the implications that stochastic resonance decoding may have for emerging post-CMOS technologies, giving particular attention to the rapidly developing fields of memristive[1] logic and ReRAMs [47]. There is currently a great deal of research focused on these topics, driven by the solid-state memory and neuromorphic computing communities. The latter community has been especially interested in memristors' native stochastic resistance-switching behavior, which holds great promise for implementing stochastic spiking neural networks [48] and Bayesian inference [49], which is closely linked to error correction. Some authors have proposed using memristors as the foundation for stochastic computing systems [3], which are closely related to stochastic decoding methods. Neuromorphic and stochastic computing are very interesting niche applications, but our approach would have more direct application to general-purpose computing architectures by facilitating reliable retrieval from ReRAM memories. Our decoding algorithms simultaneously benefit from the inherent non-determinism of memristor technology, while masking that non-determinism at the interface to other system components. Memristive devices are especially interesting since they deliver the kind of tunable non-deterministic behavior envisioned by our theory, and our theory can potentially resolve what is sometimes seen as a limiting volatility for large-scale ReRAM.

The stochastic nature of memristors is depicted in Fig. 7. A typical memristor is a thin-film device (Fig. 7-a) in which the resistance can be abruptly switched through formation and rupture of ion filaments [51]. HP reports successful switching with devices as small as $3\,\mathrm{nm} \times 3\,\mathrm{nm}$, with switching speeds above 1 GHz. Until very recently, resistance switching devices were treated as deterministic switches characterized by "pinched hysteresis" (Fig. 7-c). This behavior forms

[1]There has been some controversy over the linkage between Chua's general memristor theory and resistance-switching devices. We use the term "memristor" to refer exclusively to the empirical characteristics of thin-film switching devices.

the basis of a new crossbar logic topology based on material implication [53]. An example of implication logic is shown in Fig. 7-d, where the state of device M_Q is conditioned on that of M_P; in this example M_P is in a low-resistance state that dominates the voltage divider around M_Q, so that the applied voltage across M_Q is only 2 V, less than the threshold for switching. M_Q is supposed to retain its state in this example, but **more recent research indicates that filaments form non-deterministically when driven at *subthreshold* voltages**. Fig. 7-e shows experimental results for a memristor repeatedly pulsed at a subthreshold amplitude, causing random switching in a minority of cases. The switching probability distribution, shown in Fig. 7-f, can be adjusted by varying the pulse width and amplitude. The authors of [52] observed a very high rate of random switching for long-duration pulses; with narrow-width pulses there should be a lower rate of switching which is more difficult to observe, but still important for the reliability of a large-scale system [54].

For application in stochastic computing circuits, the probability of switching is most commonly modeled as a Poisson-like switching process, controlled by two intrinsic device parameters: a time-scale parameter τ_0, and voltage-scale parameter V_0. When the device is exposed to a subthreshold pulse of amplitude V and width t, the switching probability is expected to be $p = 1 - \exp(-t/\tau)$, where $\tau = \tau_0 \exp(-V/V_0)$. In principle, this model should allow for a precisely tuned switching probability, serving as the source of randomness in the PGDBF algorithm.

This statistical model cane be readily applied if we assume that each symbol-node processor is a standard CMOS circuit augmented by an individual memristor as a noise source. A more challenging task is to construct these modules entirely from memristor devices. To begin with, we will examine a material implication circuit like the structure shown in Fig. 7-d, where we should be able to control both deterministic and non-deterministic events by using different pulse characteristics. Circuit simulation models of stochastic switching are quite new, and mature public models have appeared only within the past year [55]. It will take some effort to build a scalable model suitable for simulating our decoder modules.

Once we have verified the concept of a memristive decoder based on implication logic, we will consider application to ReRAM storage. Stochastic switching is seen as a potential limitation for ReRAM memories, with a behavior that closely resembles the von Neumann random error model. ECC options have been suggested previously, usually relying on single-error detecting codes with decoders implemented in reliable CMOS read-out circuits [56]. When considering jointly the channel errors due to the ReRAM memory, and the internal upsets with in the memristive decoder, we should see exactly the behavior predicted by our prior research on faulty post-CMOS decoders [W2]. With our stochastic resonance decoding algorithms, it should be possible to implement a decoder within the memristor crossbar fabric local to the ReRAM array, thereby facilitating much faster readout speeds while enhancing both performance and reliability.

We will additionally validate our non-deterministic models by conducting small-scale circuit experiments using commercially available memristor samples configured to implement the basic operations of our bit-flipping algorithms. By considering established cross-bar circuit topologies and extrapolating to larger scales, we will be able to estimate the tradeoffs among energy, reliability and area overhead when using stochastic resonance decoding on short and medium-length codes.

3 Broader Impacts of the Proposed Work

International Collaboration. Together with their French collaborators, the PIs have realized over 3 Million Euros in two funded projects from French agencies, building from the Vasic's theory of fault-tolerant decoders developed under the NSF funded project CCF-0634969. Most recently, the PIs are collaborating on the 1.5 Million Euro, "NAND" project (ANR-15-CE25-0006-01) funded by the Agence Nationale de la Recherche (ANR) which supports the French part of the team until 2019, and includes more than twelve French institutions from both academia and industry. In 2012, the Vasic and Declercq founded a company (Codelucida) focusing on iterative decoder solutions based on theory developed within the NSF project.

Integration of Research and Education. The training that this research will provide to graduate students will enable them to make significant technological contributions to the communications/networking industries upon graduation. To foster integration of research and cross-disciplinary education, we plan to hold monthly seminars to form a bridge between coding and information theory, quantum computing, statistical physics and system architecture for our international partners, graduate and undergraduate students. Co-advising opportunities among the team members from the partner universities will better prepare them for careers in industry. The University of Arizona already has a dual graduate degree program with ENSEA, France, and we envision similar agreements with the universities involved in this project. The interdisciplinary nature of the proposed project will naturally foster cross-disciplinary education. This process will be aided by the rapid dissemination of research results through a special graduate seminar course on sustainable. This course will also serve as a springboard for the development of a new graduate course, with applications ranging from nanotechnologies to information theory.

Implications for Technology. Fault tolerance has been recognized as one of the biggest challenges of the emerging nanoelectronic era [57, 58] and our research can improve the performance of memory and communications systems based on imperfect materials and devices in a wide range of new nanoscale technologies which is being actively investigated for processing and storage of digital data [59–61]. It can be also used in quantum computing [62].

In concert with addressing fault-tolerance, our work is already showing promise for advancing green technologies, where the goals are to minimize environmental impact of technological progress. The so-called "digital economy" already consumes one tenth of the world's energy production, with an expanding footprint. Data centers for cloud services consume twice the energy needed to power all the homes in New York City [63]. Our work directly relaxes the burden of one of the major energy consuming components in networking equipment: the decoder. In 10GBaseT ethernet, the decoder can consume 10–30% of a port's power consumption, and a typical data center may contain thousands of such ports. Our work can potentially slash that consumption and slow the growth of the world's energy footprint.

Cooperation with industrial researchers working on error-correcting codes for data storage has already started. Vasic has been involved in the work of the Advanced Storage Industry Consortium involving major companies and selected universities around the globe. Other ongoing collaborations of the PI include researchers at Hitachi, Seagate, Western Digital, Marvell Semiconductor, Indian Institute of Science, Data Storage Institute, University of Belgrade, and Georgia Tech.

Outreach to the Community. The results obtained during this project will be disseminated through journal and conference papers, talks, and tutorials. The PIs also maintain web sites that post the latest research results. The PIs have also been actively involved in organizing conferences, special

sessions, special issues of journals, seminars, and workshops. Recent examples include, organizing the Special Session on Noisy Error Correction within Turbo Coding Symposium to be held in Brest, France, and IEEE Journal on Selected Areas in Communications, Special Issue on Communication Techniques for Channel Modeling, Coding and Signal Processing for Novel Physical Memory Devices and Systems, and IEEE Journal on Selected Areas in Communications, Special Issue on Communication Techniques for Storage Channels and Networks. Vasic also serves as a Chair of the IEEE Data Storage Technical Committee, where his responsibilities include coordination of data storage tracks at major conferences, appointing the Best Paper Award in Data Storage Committee, and providing endorsements to the IEEE Fellow Committee. In addition, Vasic regularly speaks to general audiences about data storage techology and signal processing and coding. These audiences include freshmen and high school students as well as more general audiences. Examples include a series of lectures at the Tohono o'Odham Nation Reservation, American Corner, Svetozar Markovic Highscool and Njegos Elementary School in Nis, Serbia, and Serbian Academy of Sciences and Arts, and and a lecture to the Society of Hispanic Professional Engineers. Vasic was also a lecturer at the European School of Information Theory held in Ohrid, Macedonia in 2013, sponsored by the Information Theory Society.

4 Results from Prior NSF Support

Chris Winstead is/was the PI/Co-PI on multiple NSF grants. The grant of most relevance to this proposal is *" Career: Low-energy circuits for implantable networks"* (ECCS-0954747, 2010–2015, $400K). Winstead was the PI for this research. *Intellectual Merit:* The objective was to develop micro-power signal processing solutions for wireless bio-implantable devices. We focused on developing an Ultra-Wideband (UWB) communication solution for cortical implants using mutual-inductance transcutaneous channels. Error Correction Coding (ECC) was a key focus of this project, and we explored subthreshold analog and bit-flip decoding strategies to achieve low-power operation. Winstead's currently active international collaborations grew out of this research. The NGDBF algorithm was also discovered as a by-product of this research. *Resulting Publications*: We published several articles in peer-reviewed conferences [W5–W13] and journals [W4, W14–W16]. Three additional journal articles are in review or in preparation. When possible, our articles are published Open-Access and are disseminated on our lab web site at *http://left.usu.edu* and through USU's institutional open-access document repository. When appropriate, simulation models and demonstrations are made available for public download on our site. *Broader Impacts:* So far, this project produced one PhD graduate and one MS graduate, and two additional PhD students were supported who are nearing completion. An advanced curriculum was deployed in circuits and VLSI that provides training to a growing number of students each year, with a new cohort of 36 students enrolled for the fall 2015 semester.

Bane Vasić is/was the PI/Co-PI on multiple NSF grants. The grant of most relevance to this proposal is *"CIF Medium: Iterative Decoding Beyond Belief Propagation"* (NSF CCF-0963726, 2010–2014, $675K). *Intellectual Merit:* The project develops a theoretical framework for designing iterative decoders requiring only a small number bits of message precision which can surpass floating-point belief propagation in the error floor region. *Resulting Publications*: The award has resulted in more than 20 journal papers, more than 30 conference papers, one book, one book chapter, one patent, and disclosure of three inventions. Representative publications include [V24], [V25] and [V14, V26–V30]. (The complete list of all products as well as other relevant information is given on the project

web site [V31]). *Broader Impacts:* The project has supported PhD students including Shiva Kumar Planjery, Dung Viet Nguyen, Vida Ravanmehr and Seyed Mehrdad Khatami. In 2012, the Co-PI founded a company (Codelucida) focusing on development of iterative decoder solutions based on the theory and IP [V24] developed within this project. In 2014, the company received a SBIR Phase-I Grant (NSF SBIR–1415704), and in 2015, SBIR Phase-II Grant (NSF SBIR–1534760).

5 Collaboration Plan

Expertise of Key Personnel

The proposed research program requires synergistic efforts and is based on unique expertise of the PIs and foreigin collaborators.

C. Winstead's expertise is primarily in circuit implementation of error correction methods. His past work has emphasized micro-power analog subthreshold decoders [W17–W31], digital stochastic decoders [W1, W3, W32], subthreshold bit-flipping decoders [W16] and their application to energy-constrained systems, particularly bio-compatible electronics [W8, W12, W13]. Winstead has also done some investigation into fault tolerant circuit theory [W15, W33–W35] and decoding on noisy hardware with relevance to post-CMOS electronics [W9–W11, W36, W37], including some preliminary indications of noise-enhancement in those technologies [W2].

B. Vasic's expertise is in error correction codes and data storage systems with emphasis on fault-tolerant storage systems [V1, V23, V32–V35], magnetic data storage [V36–V38], codes on graphs [V39–V42] and iterative decoding [V25, V28, V29, V29, V30, V43], energy and hardware-efficient error correction systems [V14, V27, V44] and approximate inference algorithms originating in statistical mechanics [V21, V45].

A complete list of relevant publications can be found at web pages of the PIs:

- Vasić: `http://www2.engr.arizona.edu/~vasic/`
- Winstead: `http://left.usu.edu`

The PIs will also maintain their relationships with international collaborators, who have independent sources of funding for their work in this area. Our collaborations include Prof. Emmanuel Boutillon of the Lab-STICC group at Université de Bretagne Sud, France (UBS), Profs. David Declercq and Fakhreddine Ghaffari of the ETIS Lab at ENSEA and Université Cergy-Pontoise, France, and Prof. Predrag Ivanis of the University of Belgrade, Serbia. The expertise of our collaborators is in low-complexity iterative decoding (David Declercq), digital architectures for high-speed communication links (Emmanuel Boutillon and Fakrhreddine Ghaffari) and stochastic gradient-descent algorithms and Markov chains (Predrag Ivanis).

PI Vasic has been closely collaborating with Prof. David Declercq at Cergy-Pontoise for more than eight years. Drs. Declercq and Vasic advised more than five Ph.D. students and three postdocs, published more than a dozen joint papers, two patent applications and a book chapter, established a dual degree graduate program between the University of Arizona and University of Cergy-Pontoise, and spent sabbatical leaves at collaborator's laboratory for a total duration of almost three academic years.

PI Winstead has been collaborating with Emmanuel Boutillon for about five years, leading to six joint papers and two patent applications. Our collaboration has included four PhD students, three of whom participated in international visits between our labs. Winstead spent sabbatical leave at UBS during 2013–14. In 2015, Winstead initiated collaboration with Declercq and Ghaffari in Cergy-Pontoise. Ghaffari spent one month at USU, where we investigated the ML-approaching behavior of PGDBF. We plan to maintain these productive relationships during the term of this project.

Some funds are requested to host international guests and to support foreign visits by PIs and students under this project, as part of these continuing relationships.

Project Coordination

The collaborating institutions will schedule weekly teleconference meetings, and will arrange in-person meetings on a quarterly basis, to occur roughly in September, December, March and June. These meetings will be hosted alternately at USU and UA, and when appropriate we will hold meetings at other venues such as professional conferences.

In terms of the division of effort, all project participants will participate in all objectives, but PI Winstead will have primary responsibility for design and analysis of circuits and architectures, and PI Vasic will be primarily responsible for theoretical analyses. The rough quarterly schedule of project activities is shown in Fig. 8. For each activity, the corresponding proposal section is indicated.

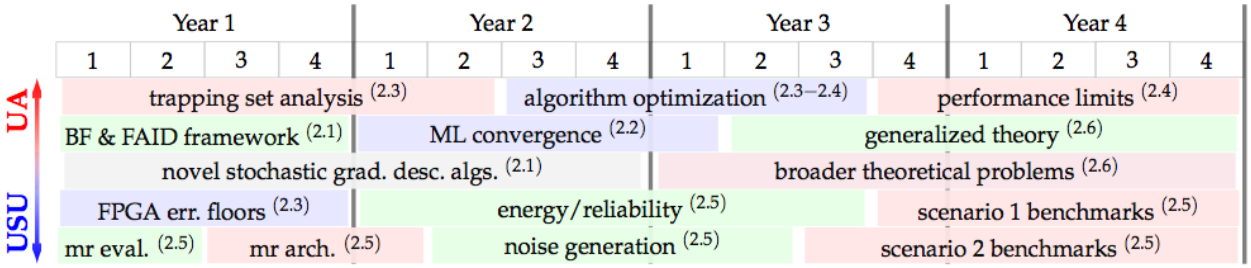


Figure 8: Project timeline showing coarse division of responsibilities by quarter. "Memristor" is abbreviated as "mr". The effort is organized so that the most well defined tasks are handled in the first two years, and the more open-ended challenges are deferred to the last two years, after we will have gained considerable knowledge and experience. Project responsibilities are loosely divided such that UA has primary responsibility for the more theoretical and algorithmic topics, while USU is responsible for applied tasks involving circuits and architectures.

To facilitate data sharing, PI Winstead will maintain remotely accessible servers in his laboratory at USU. Access priveleges will be granted to all participants at UA, ETIS and UBS. The lab already contains a secure firewalled network accessible via SSH with remote desktop using X2Go services. This configuration has been successfully used to coordinate with overseas collaborators for the past four years. Remote experiments have also been deployed in the past, and may be beneficial for some of the proposed activities. Some funds are requested for updated data storage equipment, computing server and FPGA resources to be used in this collaboration.

In addition to the on-site resources in Winstead's lab, we will make some use of cloud services. In the past, we have enjoyed good success using Skype for teleconferences, ShareLatex for jointly authored papers, and DropBox for rapid file sharing.

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The budget requested by Utah State University is outlined as follows.

Staff: PI Winstead requests one month of summer salary for project management, research and training activities. Salary for one PhD student is requested, who will be employed on a 20-hour per week basis with an annual salary of $23,345. Summer support is additionally requested in the amount of $3600 for an undergraduate participant. A 4% *cost of living adjustment is made for all salaries in each of years 2--4. The PI also anticipates a one-time 15% increase due to a rank promotion in year 2. Faculty benefits are charged initially at 45%, and graduate students at 8.2% for summer months and 0.8% during the academic year; faculty benefits increase by 0.5% and student benefits by 0.1% in each successive year. Graduate student health insurance is subsidized separately $1549 during the first year, increasing by 14% annually. The total labor and fringe benefit budget is $199,277. PhD tuition support is also requested at the full-time rate of $7071 during the first year, with anticipated annual increases of 3.55% based on recent trends.*

Equipment and Materials: We request funds to purchase an updated Xilinx Virtex development board quoted at $6995. In addition, we request funds for a standalone Xilinx software license of the same version used by our French partner, quoted at $2995, in order to coordinate our physical design work and share project files. Due to the project's aggressive computational demands, our request includes a 48-core computational workstation quoted at $9892, and a network attached RAID storage unit quoted at $610 for managing and archiving project data. Lastly we request $880 to purchase memristor samples from Knowm Inc, and an annual lab maintenance budget of $2500. The total direct costs, including equipment, materials and tuition, is $61,198.

Travel: Funds are requested to support collaborative meetings between the PIs institutions and with our French partners, and to support conference participation by the PIs and their students. We plan to hold site meetings quarterly, for a duration of four days including travel days, alternating between University of Arizona and Utah State University locations. At USU, research partners will be accommodated in graduate student housing at the rate of $20 per person per night. The current air fare rate from Tucson to Salt Lake City is $385, plus an allowance of $50 for baggage fees and $100 for ground transportation which is sufficient for taxi/parking fees and an airport shuttle from the USU campus. A meal allowance of $40 per day is requested. Assuming two participants visiting USU in two meetings per year, the annual cost is $3100.

We also request funds to support one annual site visit at the ETIS lab in Cergy-Pontoise, France. Air fare from Salt Lake City to Paris is quoted at $1420, plus a $50 allowance for baggage fees and $100 for ground transportation. Accommodations are available in student housing at the converted rate of $46.33

per person per night. A food allowance of $60 per day is suggested. If an international PhD student is recruited for the project, then a Visa approval may be required for traveling to France, which involves appearing at the consulate in San Francisco with a cost of about $400. For travel including the PI and one student, the total annual cost is $5268.62.

In order to reciprocate collaborative relationships, we request funds to host student or faculty exchange visits from our French partners, who typically travel to our US locations for a duration of one month. We propose to pay the travel and lodging costs for one visitor in each year of the project. At USU, with the graduate student housing rate of $20 per night, and the air fare price of $1420 plus baggage and ground transportation, the expected total cost is $2170 per year.

Lastly, we request funds to support travel participation by the PI and one student participant. On average, we plan to attend one international conference and two domestic conferences each year. Using last year's International Symposium on Information Theory, held in Hong Kong, as a reference for international conference costs, we anticipate air cost of $1500 per traveler, plus baggage and ground transportation of $150, and nightly hotel costs of $175, and a food allowance of $75 per day for a duration of seven days, including travel days. A faculty registration fee of $834 and student registration of $450 is typical. Then the total for two travelers is $7384 per year. It may be possible in some cases to reduce this cost, e.g. by sharing hotel rooms or ground transportation , but this is not always possible, for example travelers of different gender usually require separate hotel rooms. This brings the total annual cost for international travel, including ETIS visits, international exchanges and conference participation, to $14,822.62.

For travel to domestic conferences, a lower air fare of $500 per traveler is typical, using the upcoming Design Automation Conference in Austin, TX as a reference. Hotel rates of $112 per night are available, and a meal allowance of $50 per day is sufficient. Registration fees are similar to those quoted above. Assuming five hotel nights and two travel days, the total cost for two participants is $4474 per conference, with a total annual cost of $8948. This brings the total annual cost for domestic travel to $12,048.

Combining these requests, the total travel budget is $26,870.62 annually and for four years is $107,482.48.